**DAILY ASSESSMENT FORMAT**

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| **Date:** | **2/06/2020** | **Name:** | **Navya** |
| **Course:** | **Digital Design Using HDL** | **USN:** | **4AL17EC060** |
| **Topic:** | **FPGA Basics: Architecture, Applications and Uses**  **Verilog HDL Basics by intel**  **Verilog Test bench code to verify the design under test (DUT).** | **Semester & Section:** | **6th sem**  **A section** |
| **GitHub Repository** | **Navya-courses** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.** |

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| **Date:** | **2/06/2020** | **Name:** | **Navya** |
| **Course:** | **Python** | **USN:** | **4AL17EC060** |
| **Topic:** | **Timing your code-timeit**  **Regular Expressions**  **StrinIO** | **Semester & Section:** | **6th sem**  **A section** |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session**        **RPA Certificate** | | | |